

AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (PREVIOUSLY PRESENTED) An apparatus comprising:

a plurality of processors;

a trace circuit configured to present information at a
port for debugging software in a selected processor of said
5 processors;

a connector circuit configured to (i) couple said trace
circuit to said selected processor in response to a select signal
and (ii) transfer said information from said selected processor to
said trace circuit while said selected processor is executing said
10 software; and

a boundary scan chain connected to each of said
processors and said trace circuit.

2. (ORIGINAL) The apparatus according to claim 1,
wherein said connector circuit is further configured to transfer
data from said trace circuit to said selected processor.

3. (PREVIOUSLY PRESENTED) The apparatus according to
claim 1, wherein said connector circuit is further configured to
transfer a first test data stream received by said selected
processor through said boundary scan chain to said trace circuit.

4. (PREVIOUSLY PRESENTED) The apparatus according to claim 3, wherein said connector circuit is further configured to transfer a second test data stream from said trace circuit through said boundary scan chain to said selected processor.

5. (ORIGINAL) The apparatus according to claim 1, wherein said connector circuit comprises:

a first circuit configured to (i) transfer said information from said selected processor to said trace circuit, (ii) transfer data from said trace circuit to said selected processor, and (iii) present a predetermined logic state to said processors other than said selected processor; and

a second circuit configured to (i) transfer a first test data stream received by said selected processor to said trace circuit, (ii) transfer a second test data stream from said trace circuit to said selected processor, and (iii) present a second predetermined logic state to said processors other than said selected processor.

6. (CURRENTLY AMENDED) The apparatus according to claim 51, wherein said ~~first~~ connector circuit comprises:

a first multiplexer configured to multiplex said information from said processors to said trace circuit in response to said select signal; and

a first plurality of gates each coupled to one of said processors and configured to (i) transfer ~~said~~ data while selected

by said select signal and (ii) present ~~said~~ a predetermined logic state while not selected by said select signal.

7. (CURRENTLY AMENDED) The apparatus according to claim 6, wherein said ~~second~~ connector circuit further comprises:

a second multiplexer configured to multiplex a plurality of first test data streams received by said processors to said trace circuit in response to said select signal; and

a second plurality of gates each coupled to one of said processors and configured to (i) transfer a second test data stream while selected by said select signal and (ii) present ~~said~~ a second predetermined logic state while not selected by said select signal.

8. (ORIGINAL) The apparatus according to claim 6, wherein each of said gates comprises a logical AND gate having at least one input configured to receive said select signal.

9. (CURRENTLY AMENDED) A method for debugging software in a selected processor of a plurality of processors, comprising the steps of:

(A) coupling a trace circuit to said selected processor in response to a select signal;

(B) transferring ~~said~~ information from said selected processor to said trace circuit while said selected processor is executing said software;

(C) presenting said information received by said trace
10 circuit at a port; and

(D) connecting said processors and said trace circuit
through a boundary scan chain.

10. (ORIGINAL) The method according to claim 9, further
comprising the steps of transferring data from said trace circuit
to said selected processor.

11. (PREVIOUSLY PRESENTED) The method according to claim
9, further comprising the step of transferring a first test data
stream received by said selected processor to said trace circuit.

12. (ORIGINAL) The method according to claim 11, further
comprising the step of transferring a second test data stream from
said trace circuit to said selected processor.

13. (CURRENTLY AMENDED) The method according to claim
12, further comprising the step of presenting a predetermined logic
state to said processors other than said selected processor in
response to transferring said second test data stream.

14. (ORIGINAL) The method according to claim 13, further
comprising the step of presenting a second predetermined logic
state to said processors other than said selected processor in
response to transferring said second test data stream.

15. (ORIGINAL) The method according to claim 12, wherein said step of transferring said information comprises the sub-step of multiplexing said information in response to said select signal.

16. (CURRENTLY AMENDED) The method according to claim 15, wherein said step of transferring said second test data stream comprises the sub-step of gating said second test data stream in response to said select signal.

17. (ORIGINAL) The method according to claim 16, wherein said step of transferring said first test data stream comprises the sub-step of multiplexing said first test data stream in response to said select signal.

18. (ORIGINAL) The method according to claim 17, wherein said step of transferring said second test data stream comprises the sub-step of gating said second test data stream in response to said select signal.

19. (CURRENTLY AMENDED) An apparatus comprising:

means for coupling a trace circuit to a selected processor of a plurality of processors in response to a select signal;

5 means for transferring information from said selected processor to said trace circuit while said selected processor is executing ~~said~~ software;

means for presenting said information received by said
trace circuit at a port; and

10 boundary scan means connected to said processors and said
trace circuit.

20. (PREVIOUSLY PRESENTED) The circuit according to
claim 1, wherein said processors, said trace circuit and said
connector circuit are embedded in a single integrated circuit.